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Employing Multi-Phase DG Sources as Active Power Filters, Using Fuzzy Logic Controller

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Abstract

By placing distributed generation power sources beside a big nonlinear load, these sources can be used as a power quality enhancer, while injecting some active power to the network. In this paper, a new scheme to use the distributed generation power source in both operation modes is presented. In this scheme, a fuzzy controller is added to adjust the optimal set point of inverter between compensating mode and maximum active power injection mode, which works based on the harmonic content of the nonlinear load. As the high order current harmonics can be easily rejected using passive filters, the DG is used to compensate the low order harmonics of the load current. Multilevel transformerless cascade inverters are preferred in such utilization, as they have more flexibility in current/voltage waveform. The proposed scheme is simulated in MATLAB/SIMULINK to evaluate the circuit performance. Then, a 1kw single phase prototype of the circuit is used for experimental evaluation of the paper. Both simulative and experimental results prove that such a circuit can inject a well-controlled current with desired harmonics and THD, while having a smaller switching frequency and better efficiency, related to previous 3-phase inverter schemes in the literature.

Key words: DG Interface, Fuzzy Logic Controller, Harmonic Compensation, Multilevel Cascaded Inverter, Transformerless inverters

I. INTRODUCTION

The environmental regulations due to greenhouse gas emission, the electricity business restructuring, and the recent development in small-scale power generation are the main factors driving the energy sector into a new era. The current times sees large portions of increases in electrical energy demand. To address such a trend, a widespread installation of distributed resources, or what is known as distributed generation (DG), is being advocated.

A micro-turbine generator (MTG) unit (as a DG) is a high-speed rotating machine with the output power of up to a few hundreds of kW, and the output frequency up to kHz. As such, it is interfaced through a power electronic converter to the load system, in a conventional manner, in which the AC–DC–AC conversion system is taken for the MTG unit.

In the multilevel cascaded scheme, some H-Bridge single phase inverters are connected in a series on the output side, and fed separately on the input side. Every bridge is usually fed among a transformer and a DC link. In this type, the transformer winding impedance and current saturation restrict the input current of the DC link, and prevent the leakage current to flow.

After summing the output voltages of bridges in the series, the final output of the circuit is injected into the network through another transformer.

Designing a transformerless scheme for inverters, which injects the current to the network through a *RL* impedance, has been a subject of some studies in the literature in recent years. The major constraints of such a circuit will be the leakage current paths, overall efficiency and output current harmonics.

Many transformerless inverter topologies have been proposed in the literature, which connect the DG sources (especially PV cells) to the network. But, in this scheme, leakage current has been the major concern in most of them [1]-[6]. In [7], such a topology is controlled with a special type of double-frequency PWM method to minimize the output current ripple. An optimized full-bridge structure with two additional switches and a capacitor divider is proposed in [8], which guarantees that a freewheeling path is clamped to half input voltage in the freewheeling period. In [9], a new transformerless scheme is introduced which uses two

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inductors in current path, one for each half-cycle. This way, the current path will be separated in two half-cycles and circulating currents will be minimized. In [10], two different types of switching PWM methods are compared on a transformerless inverter, according to output current harmonics. An algorithm is proposed in order to choose the best ratings for parts of the inverter, according to total cost minimization versus the power in [11]. In [12], a method is proposed to eliminate the DC component in the output of a transformerless inverter. In [13], using two separate half H-Bridges for two half current cycles is suggested to minimize the leakage current. A new topology based on Z-source DC link is proposed in [14] to eliminate the leakage currents. In this scheme, some fast-retrieval diodes are added in a basic 3-phase inverter. In [15], some different topologies of transformerless inverters are compared according to PV galvanic isolation and leakage current paths.

In all the previous researches in the literature, the transformerless circuits are proposed just to inject the power produced by DG (especially PV cells) to network. So, a big impedance interface is always used to reduce the switching frequency of the circuit, besides holding the output current THD in an acceptable bond. But when the inverter wants to compensate the load harmonics, a big impedance may prevent the inverter current to track the reference closely.

A new scheme to use the distributed generation power source in both operation modes is presented in this paper. A fuzzy controller is proposed to adjust the optimal set point of inverter between compensating mode and maximum active power injection mode, which works based on the harmonic content of the nonlinear load. As the high order current harmonics can be easily rejected using passive filters, the DG is only used to compensate the low order harmonics of the load current. Multilevel cascade inverters are preferred in such use, as they have more flexibility in current/voltage waveform. To minimize the total cost, transformers are omitted in this circuit on output sides. Then, some proper impedances are employed in the current path. All the H-Bridges are controlled based on a multilevel hysteresis current source control system [16]. Since there is more switching in lower bridges according to hysteresis controller, separate inductors are employed for each half cycle of the current in them. This will also improve the total efficiency of the circuit in relation to fixing the big impedance interface.

This proposed scheme, including the power circuitry and the control method, can compensate some major current harmonic components of the nonlinear load (as in APFs), and inject maximum possible active power as a DG source interface, simultaneously. Using multilevel inverters, the switching frequency and losses will be lower than in usual 3-phase inverters. There will be no need to any filtering in output side.

Since there's a limitation on the total inverter current, an optimal set point between harmonic content and the main current component should be determined in current reference by the controller of the inverter. As the compensation problem is usually studied in steady state, and a nonlinear relationship is present between current *rms* value, current THD, and compensation necessity, it is hard to define a single input-output function to control the inverter. So, some simple controllers like a fixed gain or PI controller may not be good options. For example, a small load current with a big THD doesn't need compensation since the harmonic currents are small enough. But, a bigger current with a smaller THD may need compensation more.

As such, a well-designed fuzzy controller is proposed in order to evaluate the optimal set point of inverter operation. This means that the fuzzy logic controller decides how much of the current capacity of the inverter should be dedicated to compensation current reference, while the rest will go for the active power injection.

The proposed scheme is simulated in MATLAB/ Simulink to validate the circuit performance both in maximum active power injection mode, and harmonic compensation mode. Then, a 1*kw* prototype of the circuit is used to experimentally validate the same tests. As the experimental prototype is a 1*kw* low power sample, the simulations are done on a low power circuitry to be comparative.

II. PROPOSED SCHEME

A basic scheme of a cascaded multilevel inverter is shown in Fig 1. Each phase includes some H-Bridges connected in series on the output side. The total output voltage varies depending on the switching state of each bridge, which can produce 3 different states:

$$\begin{cases} 1,4:on \\ 2,3:off \end{cases} \Rightarrow V_{out} = +V_{dc}$$
$$\begin{cases} 1,4:off \\ 2,3:on \end{cases} \Rightarrow V_{out} = -V_{dc} \quad (1)$$
$$\begin{cases} 1,2:off \\ 3,4:on \end{cases} \Rightarrow V_{out} = 0$$

So, if all the bridges have the same V_{dc}, a circuit with n bridges can build up to $2n+1$ output voltage levels. It is obvious that more combinations are possible when bridges have different V_{dc}. Usually, each H-bridge is fed by a capacitor bank, and a small inductor is also employed in the current path in the series to eliminate the high frequency current ripples.

A transformerless split-inductor neutral point with a clamped three-level PV grid-connected inverter is proposed in [3], which connects the PV to network via two separate inductors. The selected inductors are small enough to hold the efficiency high. But, as a result, the switching frequency is very high. Besides, the inverter is a 3-level, so the output voltage harmonics are considerable. This may expand the

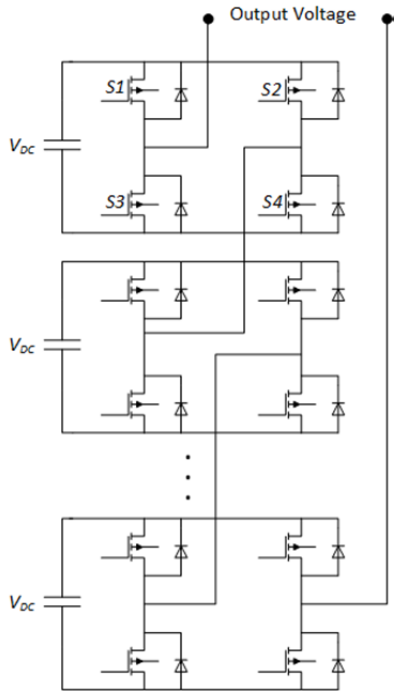

Fig. 1. Basic scheme of a cascaded multilevel inverter (one phase).

voltage harmonics to power utility. The same idea has been followed in [4]. A small interface inductor of 3mH for a small prototype is proposed, which is not practical because a high switching frequency of 20kHz is employed.

In a similar scheme, using a small inductor with high switching frequency of 20kHz is also proposed in [7], where a small filtering is used in the network side of the inverter. The same idea has been followed in [13], where a simple H-bridge inverter is used to connect the PV cell to the network. A small inductance in the series with an EMC filter is utilized as the replacement for coupling transformer. Instead, the inverter is controlled by a PWM-based switching method with the frequency of 16 kHz.

Using a 3-level inverter, we may need a big inductor to connect the inverter to the network. However, this lowers the efficiency because of the internal resistance of the inductor. Another option would be a smaller inductance in addition to a small filtering and high switching frequency.

In the proposed scheme, a seven-level inverter (as in Fig. 1) is utilized as the basic circuit. In the case of having a 3-phase AC generator as DG, each phase can be used as the source of input for each bridge (if winding terminals are available isolated). So, since all three phases of DG source are used in every phase of the inverter, there will be no circulating currents between bridges.

To limit the output current variation rate, some impedance is needed in the current path after emitting the transformer at the inverter output. If a big inductor is used, we can reduce the switching frequency in maximum power injection mode, but the inverter may not follow the current reference well enough in compensation mode. Besides, the big inductor's internal resistance lowers the efficiency.

The final topology is shown in Fig. 2, where the top inverter bridge connects the network through the main link impedance, while the lower bridges come into the current path with new impedances, unless they're in the zero state (resistors stand for inductors internal resistances). When a bridge goes into zero state, this impedance is off the current path. The inductor's energy discharges into its internal resistance through the parallel diode or into the RC snubber of the inverter switches. This way, each impedance will not be in the current path for all the working cycle, so a better efficiency will be expected. For example, Fig. 3 shows the current path through the circuit in the positive half cycle, while the bridges are in positive, negative and zero state, respectively. Note that because of the diode bridges at the input of DC link, capacitors have no way to discharge into the source side [17].

A. Limiting Inductor Determination

The limiting inductors of the circuit should be small enough, so that they don't block the current variations. As an acceptable concept, the time constant of the inductor ($\tau = L/R$) should be smaller than the time constant of the current variations in the H-Bridge. As such, if the highest harmonic order in the current reference be of order *n*, with the amplitude of $(I_n)_m$ and the hysteresis bandwidth of the certain bridge be ΔI_H, minimum time for the current to pass the band will be:

$$\begin{aligned} &(I_n)_m \sin(n\omega\Delta t) = \Delta I_H \\ &\Rightarrow \Delta t_{\min} = \frac{1}{n\omega}\sin^{-1}\left(\frac{\Delta I_H}{(I_n)_m}\right) \end{aligned} \tag{2}$$

The maximum time constant of the limiting impedance should be smaller than this time. After choosing the resistance, based on the total efficiency, this equation gives the inductance of the limiting impedance:

$$L = \frac{R}{n\omega}\sin^{-1}\left(\frac{\Delta I_H}{(I_n)_m}\right) \tag{3}$$

B. Link Inductor Determination

Since the first bridge has a tighter hysteresis band, it comes into the process first, when the current lag reaches ΔI_{H1} (the hysteresis band for the first H-bridge). This means that the first bridge changes from the zero state to positive state when the current reference passes the inverter current with ΔI_{H1}. Let the reference current be like:

$$I(t) = I_1 \sin(\omega t + \varphi_1) + I_a \sin(a\omega t + \varphi_a) + I_b \sin(b\omega t + \varphi_b) + \ldots \tag{4}$$

Assuming that the highest harmonic order under compensation be *k-th* (which has frequency of kf_o and the time period of $1/kf_o$) and that the network voltage has no harmonics, the *k-th* harmonic of DC link voltage would be:

$$(V_{dc})_q = \frac{V_{dc}}{2\pi q}(1 - \cos(q\pi)) \tag{5}$$

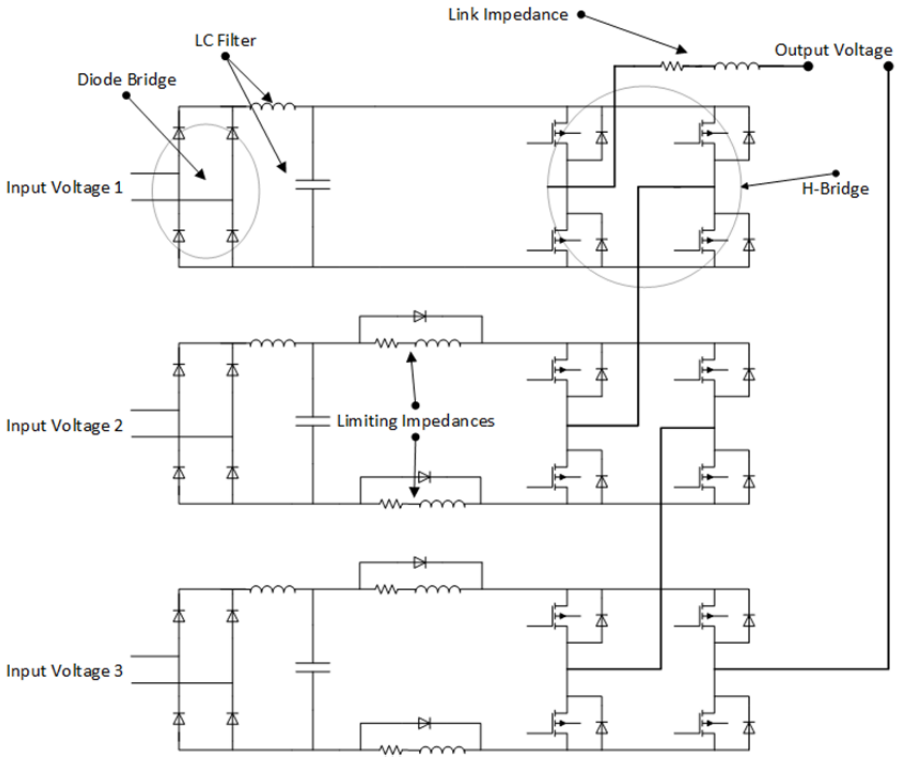

Fig. 2: Final scheme of one phase of 3-phase multilevel topology.

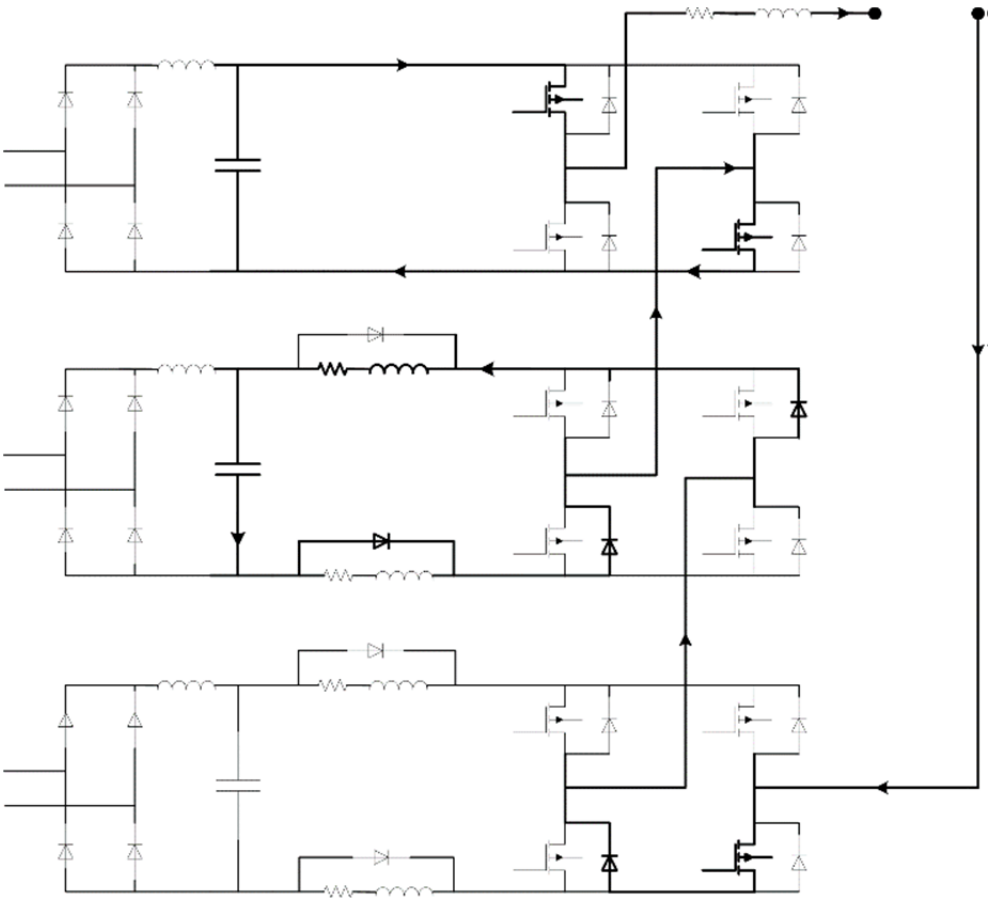

Fig. 3. The current path through the circuit in the positive half cycle, while the bridges are in positive, negative and zero state, respectively.

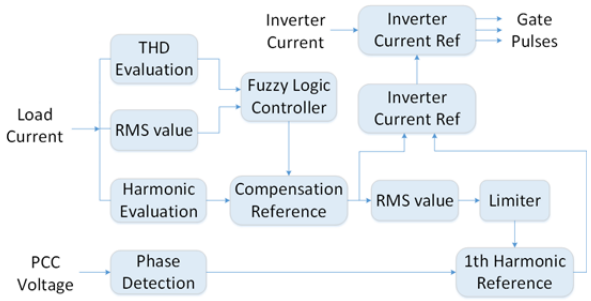

Fig. 4: Block diagram of proposed control system.

So, the *k-th* harmonic of current through the inductor will be (*k* is an odd number):

$$I_K(t) = \frac{V_{dc}/\pi k}{\sqrt{((R_{inductor})^2 + (2\pi k f_0 L)^2)}} \sin(2\pi k f_0 t) \quad (6)$$

If the rise time of the inverter current (time interval that inverter current reaches the reference) is set to $0.05/kf_o$, proper inductor can be found using (5). Note that in current injection time, the reference is not constant. If the amplitude of *k*-th current harmonic of reference is I_k, the maximum change in reference of the current in this small interval would be:

$$I_k \sin(2\pi k f_0 \frac{0.05}{kf_0}) = 0.31 I_k \quad (7)$$

After choosing the right resistor, taking efficiency into account, the inductor is determined using (5). This inductor should be small enough that the inverter current can reach the hysteresis band ΔI_{H1} and reference change of $0.31 \times I_k$ in time interval of $0.05/kf_o$:

$$\frac{V_{dc}/\pi k}{\sqrt{((R_{indcutor})^2 + (2\pi k f_0 L)^2)}} \sin(2\pi k f_0 \frac{0.05}{kf_0}) = \Delta I_{H1} + 0.31 I_k \quad (8)$$

As such, the inductor size will be:

$$L = \frac{1}{2\pi k f_0} \sqrt{\left[\frac{V_{dc}/\pi k \sin(0.1\pi)}{\Delta I_{H1} + 0.31 I_k}\right]^2 - (R_{indcutor})^2} \quad (9)$$

III. Control Algorithm

Since there is a limitation on the total inverter current, an optimal set point between harmonic content and major current component should be determined. The total harmonic distortion (THD) of the load current will be used as an index to show the load current harmonic content.

The main job of the control algorithm is to dedicate an adequate portion of the inverter current to load harmonic compensation, so that the THD of the current on the source side maintains in an acceptable bond. But when the load side THD is small enough, all the harmonic current is dedicated to active power injection. To maximize the active power injected into the network, the inverter current should be in the same phase with the phase to ground voltage at the point of common coupling. This can be obtained using park's transformation in 3-phase systems.

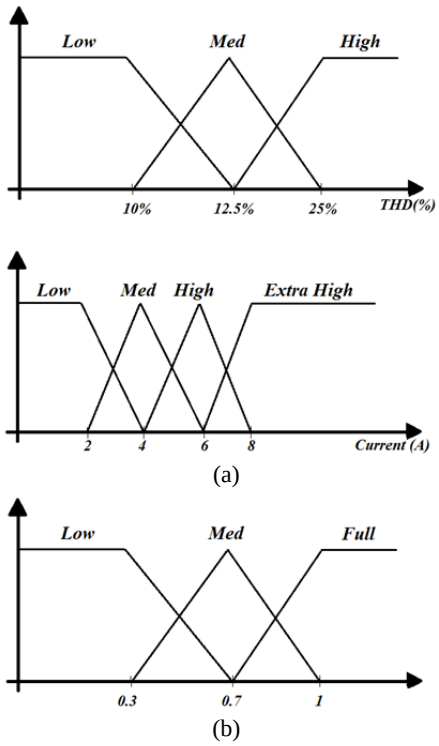

Fig. 5: Membership functions for Fuzzy controller. (a) Input. (b) Output.

The optimal set point of the inverter is determined by a variable gain, which is the output of the fuzzy logic controller. Some superior load current harmonics are evaluated first. Then, a fuzzy controller determines the harmonic compensation gain. This means that in case of low level load currents or a high load level with small THD index, the DG doesn't need to compensate the load harmonics.

Finally, the remaining part of the inverter current is dedicated to active power injection. The total block diagram scheme of the proposed control algorithm is shown in Fig. 4.

C. Fuzzy Controller Design

As mentioned before, the load current harmonic content is the main criterion to adjust the inverter's performance, which is evaluated using the THD index. As such, a current with a THD lower than 10% will be known as pure current, and has no need for compensation. A current with a THD higher than 25% is expected to be the most harmonic polluted current. Thus, it needs full compensation. Since harmonic currents are compared to a major current component in THD evaluation, the load current *rms* value is used as another input for the fuzzy controller. The membership functions of both inputs are shown in Fig. 5(a).

The output of the fuzzy controller will be the compensation gain with the membership function, as shown in Fig. 5(b). The rule base of the Mamdani fuzzy controller is summarized in Table I.

As seen in Table I, when the load current *rms* value is at a low level, there is no need for full compensation. This is

TABLE I
RULE BASE OF FUZZY CONTROLLER

RMS\THD	Low	Med	High
Low	low	low	low
Med	low	med	full
High	med	full	full
Extra	full	full	full

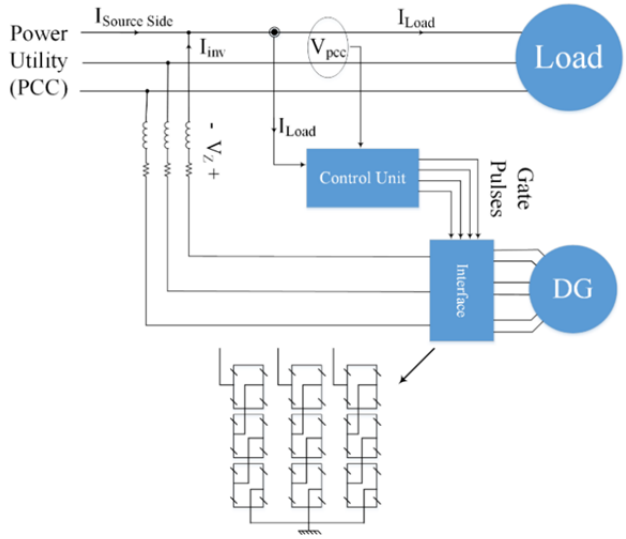

Fig. 6. Simulated system.

because harmonic currents are negligible, although the THD is big.

IV. SIMULATION RESULTS

The performance of the proposed scheme is evaluated through a simulation using *Matlab/Simulink*. The overall circuitry of the simulated system is shown in Fig 6. As seen in the figure, the network voltage at the point of common coupling uses 220 volts (phase to ground voltage peak=310 Volts). An inductive load of *R=5 Ohms* and *L=12 mH*, fed by a diode bridge, is used as the nonlinear load. The single phase inverter circuit is composed of three cascaded bridges. The hysteresis controller bandwidths are set to:

$\Delta I_1 = 0.1\ Amp\ ;\ \Delta I_2 = 0.3\ Amp\ ;\ \Delta I_3 = 0.5\ Amp\ .$

Four major harmonics of the load current are driven to be compensated. As the circuit is a single phase, triple order harmonics are included in the compensation. As such, the highest order harmonic to be compensated is *k=9*, in which its maximum magnitude is I_K*=2 A*. The maximum current capability of the inverter is set to 10 *Amp (rms)*. Thus, maximum power injection capacity would be:

$$P_{\max} = 220 \times 10 = 2.2\ \ kW \tag{10}$$

The total resistance in the current path sets in R_{Link}

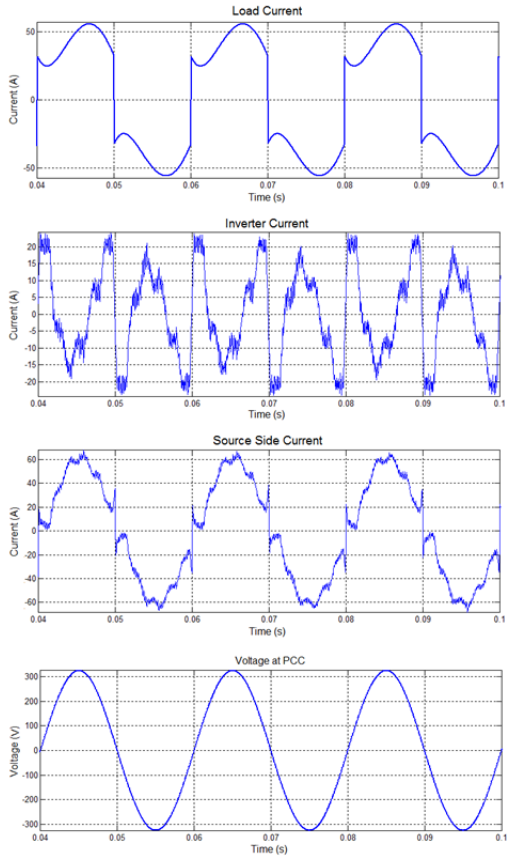

Fig. 7. System currents in non-linear load compensation mode (phase A).

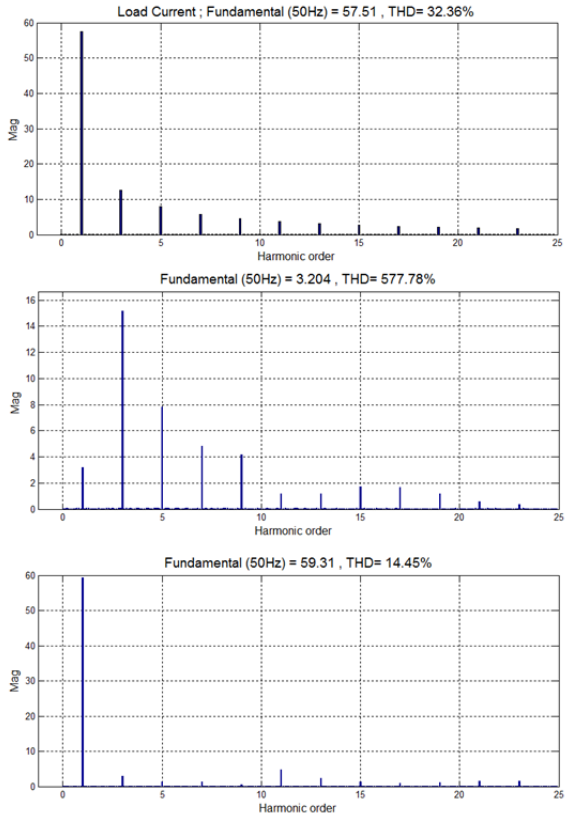

Fig. 8. FFT analysis results for currents shown in Fig. 7.

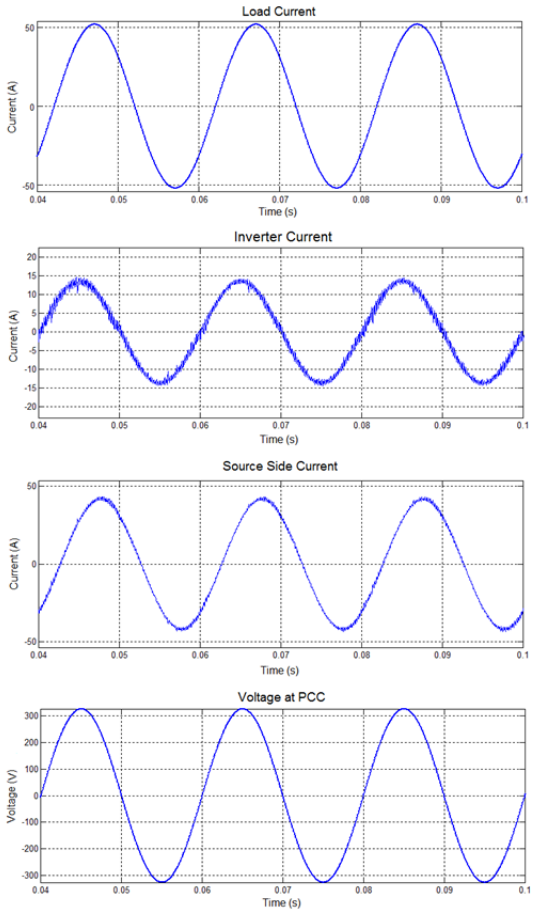

Fig. 9. System's performance under Maximum Power Injection mode (phase A).

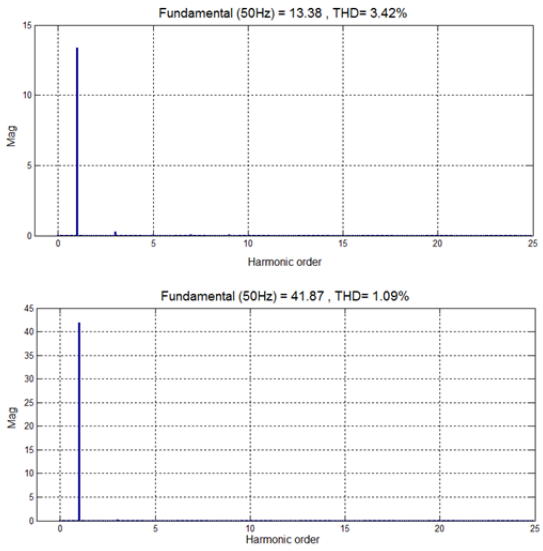

Fig. 10. FFT analysis results for currents shown in Fig. 9.

$_{inductor}$*=0.2 Ohms* and $R_{limit\ inductor}$*=0.1 Ohms*. This would make the total efficiency to be over 0.98% (neglecting the switching losses).

The link inductor of the first H-Bridge is determined to be *L=11 mH* using (8). On the other hand, the maximum capacitor bank size will be *C=1200 uf* using (11). Fig. 7

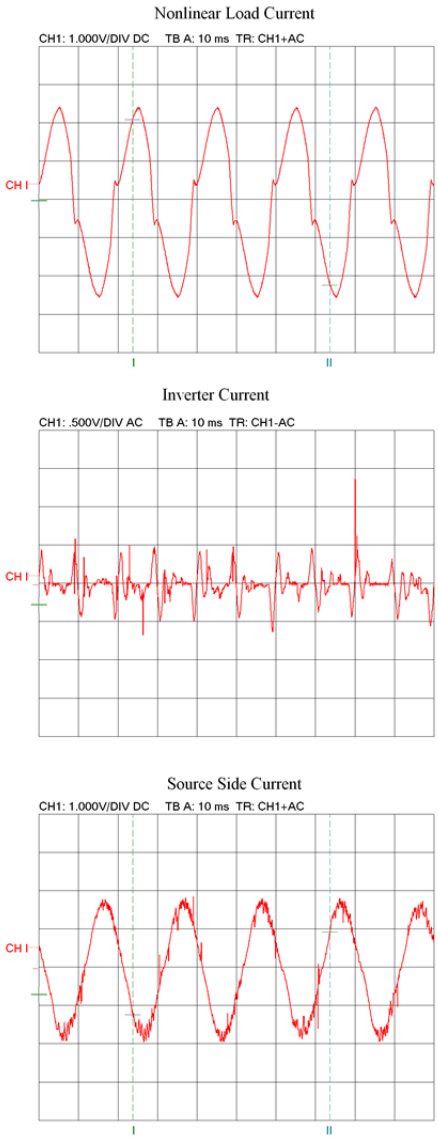

Fig. 11. Experimental results for a single phase 1 kW prototype in compensation mode (K_c*=0. 925*) (1 Volts= 10 Amp).

shows the system performance in compensation mode. Because of the nonlinear nature of the load, most of the inverter current capability has been assigned to compensate the harmonics. As the FFT analysis in Fig. 8 shows, four major harmonics in the load current are considerably compensated, while the active power injected by inverter is reduced to:

$$P = 220 \times 3.204 / \sqrt{2} = 498 \quad w$$

As another validation test, the load is substituted with a linear *RL* impedance of *R=5 Ohms* and *L=12 mH* (diode bridge is omitted). Fig. 9 shows the system performance under the new conditions, where the inverter current has no remarkable low order harmonics, while the active power injection is in the highest level. Figure 10 shows the FFT analysis for currents in Fig. 9. It can be seen that the inverter current has an acceptable THD. Such current is in the same phase with the phase to ground voltage at the point of

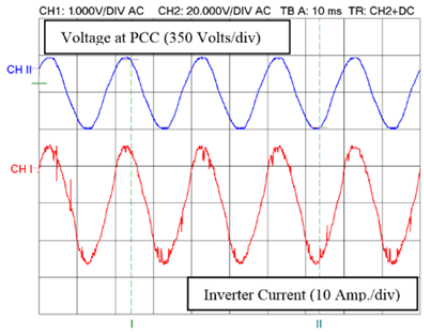

Fig. 12. Experimental results in maximum power injection mode (K_c=*0.002*).

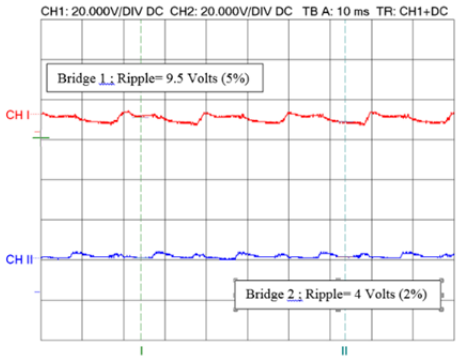

Fig. 13. DC link voltages in maximum power injection mode (experimental results).

common coupling.

V. Experimental Results

To validate the numerical and simulation results, some experiments are done on a *1kw* single phase prototype (details included in the appendix). The load is an *RL* impedance fed by a diode bridge. Figure 11 shows the system performance under compensation mode. As the prototype is a single phase circuit, triple-order harmonics are included in the compensation process. It can be seen that the harmonic content in the current on the source side is much less than the load current. This is becuase the THD was reduced from 28% in the load side to almost 11% in the source side. The source side would, then, have no need for any filtering, because it improves enough with the 3-phase transformers in the network side. The major harmonic component has been reduced, so that the compensation capability of the circuit is highlighted.

Now, in another experiment, the diode bridge is removed from the load current path, while the load has changed into a pure linear *RL* impedance. Figure 12 shows the performance in maximum power injection mode, where the current is synchronized well with the voltage, and the harmonic content in the inverter current is acceptable (THD=7.5%). Figure 13 shows the DC voltages of up-level H-Bridges in maximum power injection mode, where the DC link capacitors discharge more. As seen in the figure, there is an obvious ripple in the DC link voltages. This can be improved by using higher DC link rail voltages or using bigger size capacitors.

VI. Conclusion

This paper introduced a new transformerless cascaded multi-level inverter scheme. In this scheme, the circuit is used to connect the DG sources to the power utility. By emitting the transformers both in input and output side, the total cost is reduced, which will be the largest advantage of the proposed scheme, aside from the very acceptable harmonic content. An optimized formulation was followed to derive the best choices for each part of the circuit. Then, a supplementary control loop was added to enable the system to compensate the load current harmonics, if needed. A fuzzy logic controller was proposed to regulate the compensating operation of the inverter. The simulation of the system performance using *Matlab/Simulink* showed the perfect and accurate outputs achieved by the designed circuit. The experimental tests on a laboratory prototype proved that the system can improve the load harmonics distortion in the source side, and inject maximum possible active power simultaneously.

Appendix

The experimental single phase prototype system used in this research is shown below, using these elements:

R_{limit}=0.12 Ohms
Capacitor size in each bridge= 660 uF
Filter Inductors= 100 uH
Link Inductors= 12 mH ; 6 mH ; 1 mH
DC rail voltages= 3x100 Volts
Inductors internal resistances= 0.1 Ohms

References

[1] X. Shaojun, "Transformerless split-inductor neutral point clamped three-level PV grid-connected inverter," *IEEE Trans. Power Electron.*, Vol. 27, No. 4, pp 1799-1808, Apr. 2012.
[2] K. Sun, L. Feng, H. Wu, and Y. Xing, "A family of neutral point clamped full-bridge topologies for transformerless photovoltaic grid-tied inverters," *IEEE Trans. Power Electron.*, Vol. 28 , No. 2 , pp. 730-739, Feb. 2013.
[3] S. Xie, Y. Chen, and R. Huang, "An optimized transformerless photovoltaic grid-connected inverter," *IEEE Trans. Ind. Electron.*, Vol. 58 , No. 5, pp. 1887-1895, May 2011.
[4] H. Xiao and S. Xie, "Leakage current analytical model and application in single-phase transformerless photovoltaic grid-connected inverter," *IEEE Trans. Electromagn. Compat.*, Vol. 52, No. 4, pp. 902-913, Nov. 2010.
[5] R. Teodorescu, P. Rodríguez, G. Vázquez, and E. Aldabas, "A new high-efficiency single-phase transformerless PV inverter topology," *IEEE Trans. Ind. Electron.*, Vol. 58, No. 1, pp. 184-191, Jan. 2011.

[6] J. Lopez, P. Sanchis, and L. Marroyo, "Transformerless inverter for single-phase photovoltaic systems," *IEEE Trans. Power Electron.*, Vol. 22 , No. 2, pp. 693-697, Mar. 2007.
[7] G. Yunjie, W. Li, Y. Zhao, B. Yang, Ch. Li, X. He, "Transformerless inverter with virtual DC bus concept for cost-effective grid-connected PV power systems," *IEEE Trans. Power Electron.*, Vol. 28, No. 2, pp. 793-805, Feb. 2013.
[8] R. Gonzalez, E. Gubia, J. Lopez, and L. Marroyo, "Transformerless single-phase multilevel-based photovoltaic inverter," *IEEE Trans. Ind. Electron.*, Vol. 55 , No. 7, pp. 2694-2702, Jul. 2008.
[9] J. Dominic,J. S. Lai, C. L. Chen, T. LaBella, B. Chen, "High reliability and efficiency single-phase transformerless inverter for grid-connected photovoltaic systems," *IEEE Trans. Power Electron.*, Vol. 28, No. 5, pp. 2235-2245, May 2013.
[10] W. Li, Y. Gu, W. Cui, and X. He, "Improved transformerless inverter with common-mode leakage current elimination for a photovoltaic grid-connected power system," *IEEE Trans. Power Electron.*, Vol. 27, No. 2, pp. 752-762, Feb. 2012.
[11] E. Koutroulis, "Methodology for the optimal design of transformerless grid-connected PV inverters," *IEEE Trans. Power Electron.*, Vol. 27 , No. 2 , pp. 752-762, Sep. 2012.
[12] D. J. Atkinson, C. M. Johnson, T. D. Abeyasekera, "Auto-calibrating DC link current sensing technique for transformerless, grid connected, H-bridge inverter systems," *IEEE Trans. Power Electron.*, Vol. 21 , No. 5, pp. 1385-1393, Sep. 2006.
[13] S. V. Araujo, P. Zacharias, and R. Mallwitz, "Highly efficient single-phase transformerless inverters for grid-connected photovoltaic systems," *IEEE Trans. Ind. Electron.*, Vol. 57, No. 9, pp. 3118-3128, Sep. 2010.
[14] M. C. Cavalcanti, P. E. P. Ferraz, F. A. S. Neves, E. C. dos Santos, and J. H. G. M. da Silva, "Modulation for three-phase transformerless Z-source inverter to reduce leakage currents in photovoltaic systems," *IEEE Trans. Ind. Electron.*, Vol. 58 , No. 12, pp. 5385-5395, Dec. 2011.
[15] M. Liserre, R. Teodorescu, C. Klumpner, and M. Sumner, "Evaluation of three-phase transformerless photovoltaic inverter topologies," *IEEE Trans. Power Electron.*, Vol. 24 , No. 9, pp. 2202-2211, Sep. 2009.
[16] K. A. Corzine, "A hysteresis current-regulated control for multi-level drives," *IEEE Trans. Energy Convers.*, Vol. 15, No. 2, pp. 169-175, Jun. 2000.
[17] M. Ebadi, M. Joorabian, and J. Shokrollahi Moghani, "Multilevel cascaded transformerless inverter for connectingdistributed-generation sourcestonetwork," *IET Power Electronics*, Vol. 7, No. 7, pp. 1691-1703, Jul. 2014.

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